ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes a data buffer for inputting/outputting data from/to an exterior of the device, a plurality of DRAM cell array blocks, an SRAM redundancy cell which is situated around each of the plurality of DRAM cell array blocks, a fuse circuit which stores therein an address of a defect memory cell in the DRAM cell array blocks, a comparison circuit which compares an input address with the address stored in the fuse circuit, and an I/O bus which couple the SRAM redundancy cell to the data buffer in response to an address match found by the comparison circuit.